



## Description

The SYFR8128FK is a 4.5~5.5V 1Mbit nonvolatile memory module employing advanced ferroelectric devices. A ferroelectric random access memory or FRAM is nonvolatile but operates similar to SRAM. Unlike SRAM, FRAM requires no additional battery backup circuitry thus reducing costs and increasing reliability. FRAM is best suited to environments where frequent rapid writes are required.

The module offers cycle times of 150/160/180ns for both read and writes. 10 year data retention is standard and the device can be screened to Commercial and Industrial temperature grades.

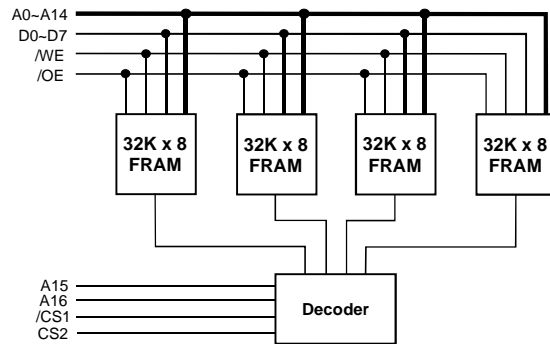
## Features

- 1 Mbit 4.5~5.5V FRAM.
- Non volatile with fast write time.
- Access time of 85/100/120ns.
- Cycle time of 150/160/180ns.
- Equal Read/Write cycle time.
- Operates similar to SRAM without the need for a battery backup circuit.
- Low power consumption.
- Address latching on active chip enables.
- Almost unlimited Read/Write endurance.
- 10 years data retention.
- Commercial & Industrial temperature grades.
- Hardware data protection circuitry.
- Data polling for end of write condition is unnecessary.
- Pin Definition compatible with 128K x 8 FRAM.

## Package Details

32 Pin Dual in Line Package (DIP) :  
Max. Dimensions (mm) - 46.00 x 15.92 x 7.00

## Block Diagram



## Pin Definition

NC	1	32	VCC
A16	2	31	A15
A14	3	30	CS2
A12	4	29	/WE
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	/OE
A2	10	23	A10
A1	11	22	/CS1
A0	12	21	D7
D0	13	20	D6
D1	14	19	D5
D2	15	18	D4
GND	16	17	D3

### Pin Functions

A0~A16	Address Inputs
D0~D7	Data Input/Output
/CS1,CS2	Chip Selects
/OE	Output Enable
/WE	Write Enable
VCC	Power (+5.0V)
GND	Ground

## Absolute Maximum Ratings<sup>(1)</sup>

Parameter	Symbol	Min	Max	Units
Voltage on any pin relative to GND	$V_T$	-0.5	7.0	V
Storage Temperature	$T_{STG}$	-55	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+0.3$	V
Input Low voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C

## DC Electrical Characteristics ( $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ )

Parameter	Symbol	Test Condition	Min	Max	Units
Input Leakage Current	$I_{LI}$	$V_{IN} = G_{ND}$ to $V_{CC}$	-	40	mA
Output Leakage Current	$I_{LO}$	$V_{OUT} = G_{ND}$ to $V_{CC}$	-	40	mA
Operating Supply Current	$I_{CC}$	$V_{CC}=5.5\text{V}$ , $I_{OL}=0\text{mA}$ , $f=f_{MAX}$ , Min Cycle.	-	40	mA
Standby Supply Current					
Input level - TTL	$I_{SB1}$	$V_{CC}=5.5\text{V}$ , $/CS1=V_{IH}$ , $CS2 =V_{IL}$ , $I_{OL}=0\text{mA}$ , $f=f_{MAX}$ , Static Inputs	-	12	mA
Input level - CMOS	$I_{SB2}$		-	4	mA
Output Voltage Low	$V_{OL}$	$I_{OL} = -4.2\text{mA}$	-	0.4	V
Output Voltage High	$V_{OH}$	$I_{OH} = -2.0\text{mA}$	2.4	-	V

## Capacitance ( $V_{CC}=5V\pm 10\%$ , $T_A=-25^\circ\text{C}$ , $f=1\text{MHz}$ )

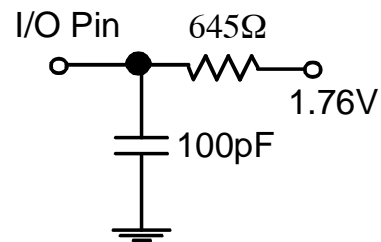
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Capacitance	$C_{IN}$	$V_{IN} = 0V$	-	-	26	pF
Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	-	-	34	pF

Note: These parameters are calculated not measured

## Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 5ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- $V_{CC} = 5V\pm 10\%$

## Output Load



## Operating Modes

/CS1	CS2	/OE	/WE	Mode
H	X	X	X	Standby/Precharge
X	L	X	X	Standby/Precharge
↘	H	X	X	Latch Address
L	↗	X	X	Latch Address
L	H	L	H	Read
L	H	X	L	Write

## Data Retention

Parameter	Min	Units	Notes
Data Retention	10	Years	1

### Notes

The relationship between retention, temperature, and the associated reliability level is characterized in a separate reliability report.

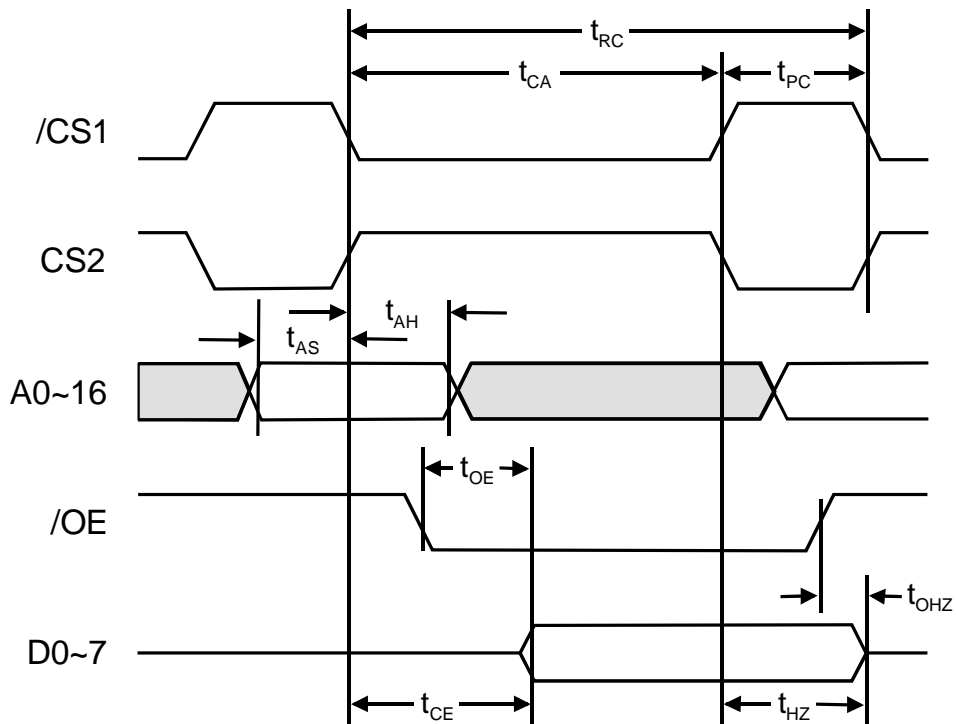
**Read Cycle** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

		85		10		12		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Chip Enable Access Time	$T_{CE}$	-	85	-	100	-	120	ns
Chip Enable Active Time	$T_{CA}$	85	10,000	100	10,000	120	10,000	ns
Read Cycle Time	$T_{RC}$	150	-	160	-	180	-	ns
Precharge Time	$T_{PC}$	60	-	60	-	60	-	ns
Address Setup Time	$T_{AS}$	5	-	5	-	5	-	ns
Address Hold Time	$T_{AH}$	25	-	25	-	25	-	ns
Output Enable Access Time	$T_{OE}$	-	10	-	10	-	10	ns
Chip Enable to Output High-Z	$T_{HZ}$	-	30	-	30	-	30	ns
Output Enable to Output High-Z	$T_{OHZ}$	-	15	-	15	-	15	ns

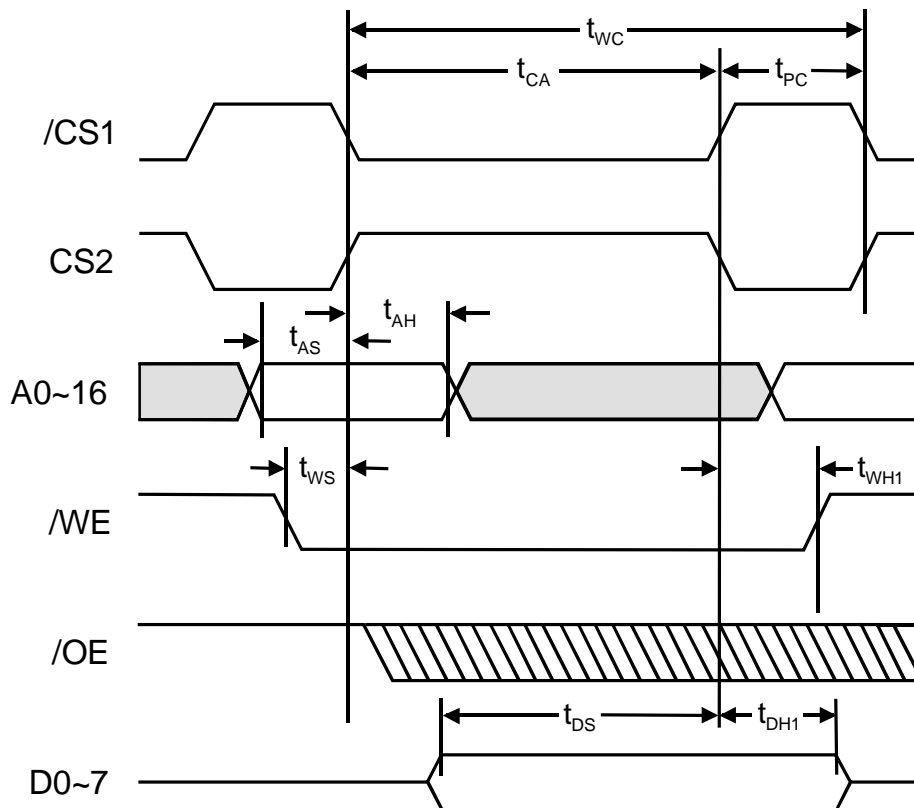
**Write Cycle** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

		85		10		12		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Chip Enable Active Time	$T_{CA}$	85	10,000	100	10,000	120	10,000	ns
Chip Enable to Write High	$T_{CW}$	85	-	100	-	120	-	ns
Write Cycle Time	$T_{WC}$	150	-	160	-	180	-	ns
Precharge Time	$T_{PC}$	60	-	60	-	60	-	ns
Address Setup Time	$T_{AS}$	5	-	5	-	5	-	ns
Address Hold Time	$T_{AH}$	25	-	25	-	25	-	ns
Write Enable Pulse Width	$T_{WP}$	40	-	50	-	60	-	ns
Data Setup	$T_{DS}$	30	-	40	-	50	-	ns
Data Hold (/CS1, CS2 Controlled)	$T_{DH1}$	20	-	20	-	20	-	ns
Data Hold (/WE Controlled)	$T_{DH2}$	5	-	5	-	5	-	ns
Write Enable Low to Output High Z	$T_{WZ}$	-	15	-	15	-	15	ns
Write Enable High to Output Driven	$T_{WX}$	10	-	10	-	10	-	ns
Chip Enable to Output High-Z	$T_{HZ}$	-	25	-	25	-	25	ns
Write Setup	$T_{WS}$	0	-	0	-	0	-	ns
Write Hold (/CS1, CS2 Controlled)	$T_{WH1}$	15	-	15	-	15	-	ns
Write Hold (/WE Controlled)	$T_{WH2}$	0	-	0	-	0	-	ns

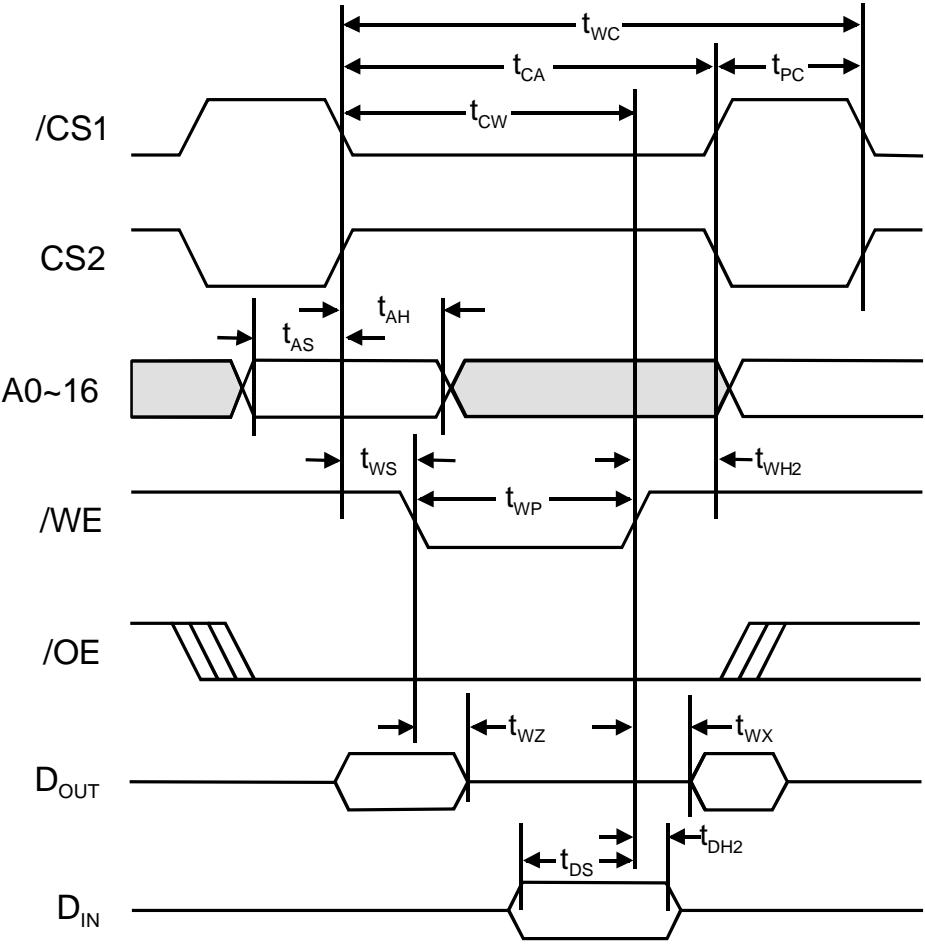
### Read Cycle



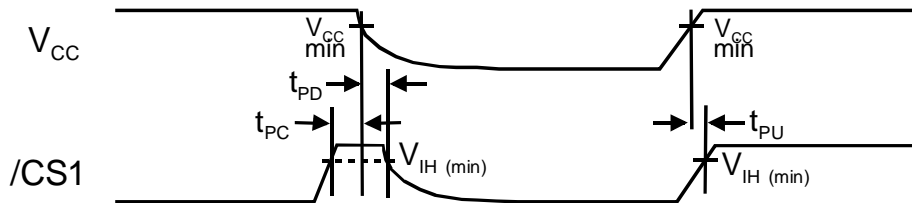
### Write Cycle - $/CS1$ , $CS2$ Controlled



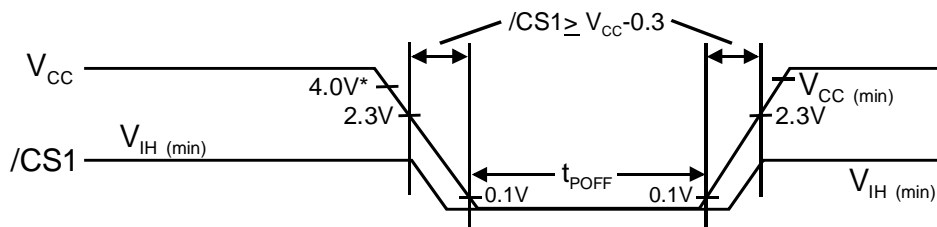
**Write Cycle - /WE Controlled**



### Power Cycle Timing



### Power Down Sequence



\* $V_{CC}$  brownout limit. Once the power supply voltage goes below this limit,  $V_{CC}$  must go to  $V_{CC(off)}$

### Power Cycle Timing ( $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CC} = 4.5V$ to $5.5V$ )

Symbol	Parameter	Min	Max	Units
$T_{PU}$	$V_{CC(min)}$ to first Access Start	1	-	mS
$T_{PD}$	Last Access Complete to $V_{CC(min)}$	0	-	mS
$T_{POFF}$	Power Off Time	1	-	mS
$V_{CC(Off)}$	Power Off Voltage	-0.1	0.1	V

#### Notes

Anytime that the power to the device ( $V_{CC}$ ) drops below 4.0 volts, the power supply must be taken to 0 Volts (+0.1 Volts) for a minimum time of 1.0 microseconds  $t_{POFF}$  before power is restored to the device. It is recommended that the  $V_{CC}$  pin be actively driven to ground through a low impedance path to ensure reliable power-up operation.

## Memory Operation

The SYF8128FK is a byte-wide FRAM organized as 128K x 8. The module is nonvolatile via its unique ferroelectric process. All data written to the device is immediately stored with no delay. Functionally the module operates similar to SRAM devices but is nonvolatile and addresses are latched on the falling edge of /CS1 or the rising edge of CS2.

Access times are the same for read and write cycles. Writes occur immediately and it is not necessary to poll the device as with traditional EEPROM devices. A Pre-Charge operation is part of every memory cycle. Therefore, access times and cycle times are not equal as with SRAM. The FRAM devices on the module feature a limited low voltage protection circuit. This prevents access when  $V_{CC}$  falls lower than the specified operating voltage range. It is the user's responsibility to ensure  $V_{CC}$  is within the data sheets tolerance to prevent incorrect operation.

## Read Operation

A read operation begins on the falling edge of /CS1 or the rising edge of CS2. Both Chip Select signals must be active to initiate a read cycle. At this time address bits are latched and the memory cycle begins. Once started a full memory cycle must be completed internally regardless of the state of the Chip Select signals. Data becomes available on the bus after the access time has been satisfied. After the address has been latched, the address may change providing the address hold parameter has been satisfied. Any change in address will not effect the module once the minimum address hold time has elapsed. When /OE goes low the data bus is driven. Valid data appears after the access time has been satisfied. If /OE is asserted prior to completion of the memory access, the data bus will be driven when valid data is available. This feature minimises supply current transients due to invalid data. When /OE is inactive the data bus remains tri-stated.

## Write Operation

A write operation requires the same time as a read cycle. As with read cycles, both Chip Select signals must be active to initiate a memory write. The device supports both Chip Select controlled writes (/CS1, CS2) or Write Enable controlled writes (/WE). In all cases, the address is latched on the falling edge of /CS1 or the rising edge of CS2.

In a Chip Select controlled write, the /WE signal is asserted prior to the beginning of the memory cycle (/WE is low before /CS1 goes low or CS2 goes high whichever is the later). Once the write cycle has been initiated the data bus will not be driven regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins when both Chip Selects are active (/CS1 goes low or CS2 goes high whichever is the later) and /WE goes low. /WE is asserted after the Chip Selects. In this case the memory cycle begins as a read and the data bus is driven according to the state of /OE until /WE goes low. The timing waveforms for both /CS1, CS2 and /WE initiated write cycles are shown in the Timing waveforms section of the datasheet.

Write access begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or when either of the Chip Select signals goes inactive, whichever is first. Data set-up time, as shown in the write timing waveforms, indicates the interval during which data cannot change prior to the end of a write access.

As there is no write delay, any operation including read or write can immediately follow a write cycle.

## Endurance

Internally, a FRAM operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on array of rows and columns. Each read or write access causes an endurance cycle for an entire row. A row is 32 bits wide. Every 4-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, FRAM offers substantially higher write endurance than other nonvolatile memories. The rated endurance limit of  $10^{10}$  cycles will allow 30 accesses per second to the same row for over 10 years.

## Pre-charge Operation

The Pre-Charge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory access and a Pre-Charge. The Pre-Charge is user initiated by making one of the Chip Select signals ( $/CS1$  or  $CS2$ ) inactive until the Pre-Charge time is satisfied. Chip select signals cannot be active indefinitely as Pre-Charges must occur. Therefore, the device has a maximum  $/CS1$ ,  $CS2$  active time which cannot be exceeded.

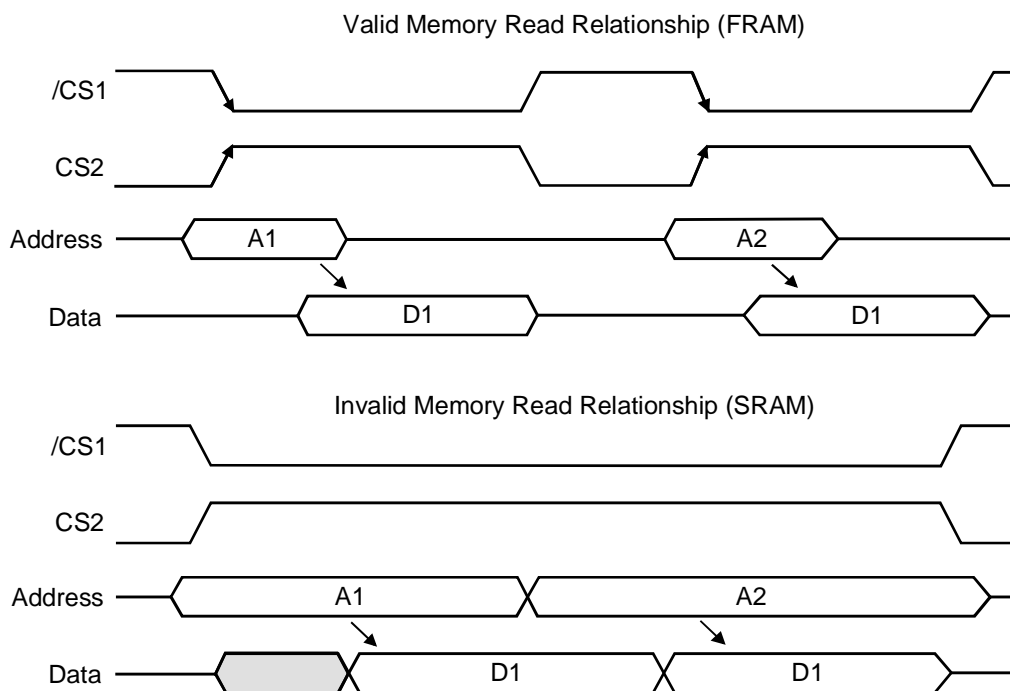
## Applications

As the module is nonvolatile RAM it is superior to most battery backed SRAM applications. The device features unlimited endurance unlike other the majority of other nonvolatile products.

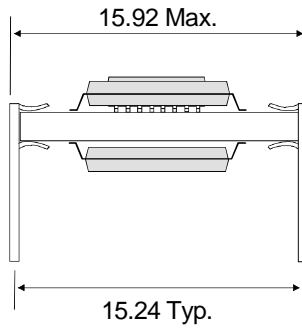
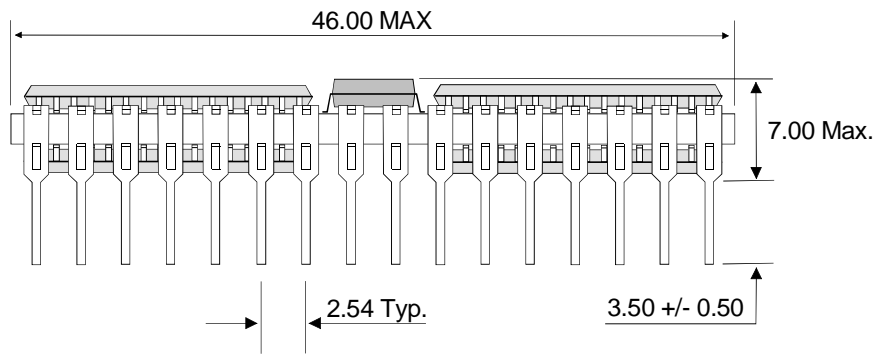
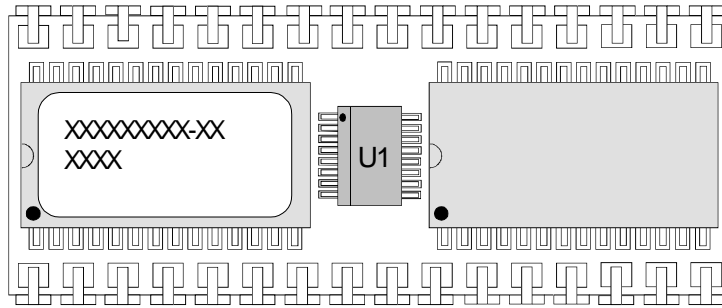
## FRAM design considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, the devices latch the addresses on both Chip Selects going active. This allows the address to change during the memory cycle. For this reason Chip Select signals must not be grounded as can be done with SRAM. Users modifying existing designs to use FRAM should examine memory controllers for timing compatibility of addresses and control lines. Each memory access must have Chip Select transitions and in many cases this is the only change required. For comparison, the diagram below shows the signal relationships for both SRAM and FRAM. Chip Select strobing is required for address latching and Pre-Charges.

Another design consideration relates to the level of  $V_{CC}$  during operation. Battery-backed SRAM systems are forced to monitor  $V_{CC}$  in order to switch to battery backup. They typically block access below a certain  $V_{CC}$  level in order to prevent loading the battery with current demand from an active SRAM device. The user can abruptly cut off from the access to nonvolatile memory in a power down situation with no warning or indication. FRAM memories do not need this system overhead. The memory will not block access at any  $V_{CC}$  level. However, the user should ensure the processor does not access the memory when  $V_{CC}$  is out of tolerance. The common practice of holding the processor in a reset condition when  $V_{CC}$  drops is adequate.

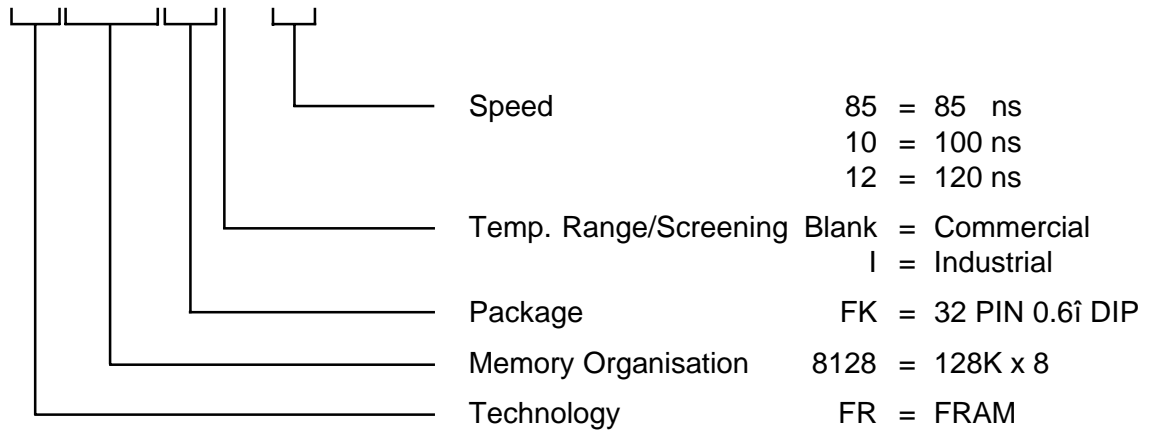


### 32 Pin 0.6" Dual In Line Package



## Ordering Information

SYFR8128FKI - 85



**Note :**

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.