

# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES



## 512K x 8 SRAM MODULE

### SYS8512FK-20/25/35/45

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#### Description

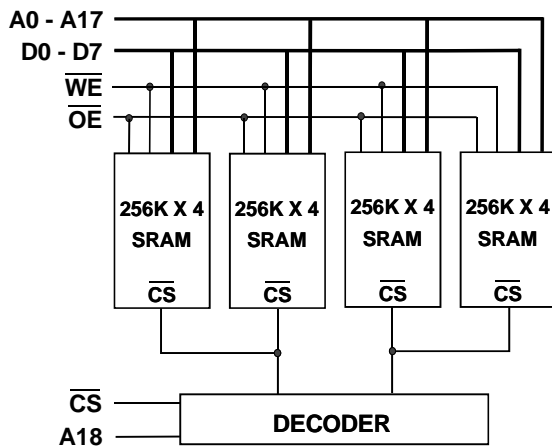
The SYS8512FK is plastic 4M Static RAM Module housed in a standard 32 pin Dual-In-Line package organised as 512K x 8. The module utilises fast 256Kx4 SRAMs housed in SOJ packages, and uses double sided surface mount techniques to achieve a very high density module.

The module has Chip Select, Write Enable and Output Enable control inputs; the Output Enable pin allows faster access times than address access during a Read Cycle.

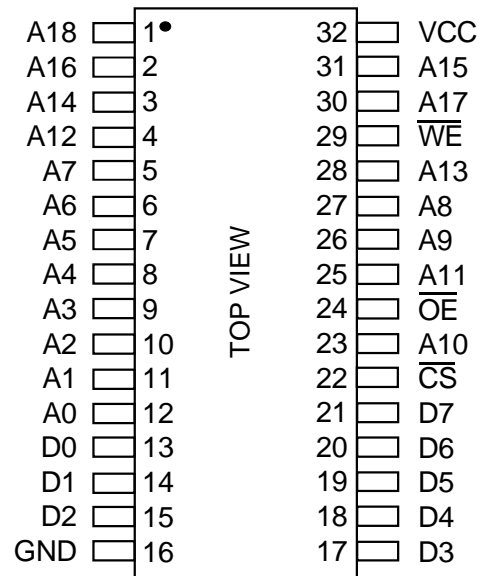
#### Features

- Access Times of 20/25/35/45 ns.
- 32 Pin 0.6" Dual-In-Line package with JEDEC compatible pinout.
- 5 Volt Supply  $\pm 10\%$ .
- Low Power Dissipation:  
Average (min cycle) 2.42W (maximum).  
Standby -L (CMOS) 44mW (maximum).
- Completely Static Operation.
- Equal Access and Cycle Times.
- All Inputs and Outputs Directly TTL Compatible
- On-board Supply Decoupling Capacitors.

#### Block Diagram



#### Pin Definition



#### Pin Functions

Address Inputs	<b>A0 - A18</b>
Data Input/Output	<b>D0 - D7</b>
Chip Select	<b><math>\overline{CS}</math></b>
Write Enable	<b><math>\overline{WE}</math></b>
Output Enable	<b><math>\overline{OE}</math></b>
Power (+5V)	<b>V<sub>cc</sub></b>
Ground	<b>GND</b>

#### Package Details

Plastic 32 pin 0.6" Jedec DIP

**DC OPERATING CONDITIONS****Absolute Maximum Ratings** <sup>(1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to $V_{SS}$	$V_T^{(2)}$	-0.3	-	7.0	V
Power Dissipation	$P_T$	-	2.5	-	W
Storage Temperature	$T_{STG}$	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2)  $V_T$  can be -2.0V pulse of less than 10ns.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature (Commercial)	$T_A$	0	-	70	°C
(Industrial)	$T_{AI}$	-40	-	85	°C

**DC Electrical Characteristics** ( $V_{CC}=5V\pm 10\%$ )  $T_A$  0 to 70 °C

Parameter	Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current Address, $\overline{OE}$ , $\overline{WE}$	$I_{LI}$	$0V \leq V_{IN} \leq V_{CC}$	-8	-	8	$\mu A$
Output Leakage Current	$I_{LO}$	$\overline{CS} = V_{IH}, V_{IO} = GND \text{ to } V_{CC}$	-40	-	40	$\mu A$
Operating Supply Current	$I_{CC1}$	Min. Cycle, $\overline{CS} = V_{IL}, V_{IL} \leq V_{IN} \leq V_{IH}$	-	-	440	mA
Standby Supply Current TTL levels	$I_{SB1}$	$\overline{CS} = V_{IH}$	-	-	246	mA
CMOS levels	$I_{SB2}$	$\overline{CS} \geq V_{CC}-0.2V, 0.2 \leq V_{IN} \leq V_{CC}-0.2V$	-	-	60	mA
-L Version (CMOS)	$I_{SB3}$	$\overline{CS} \geq V_{CC}-0.2V, 0.2 \leq V_{IN} \leq V_{CC}-0.2V$	-	-	8	mA
Output Voltage	$V_{OL}$	$I_{OL} = 8.0mA$	-	-	0.4	V
	$V_{OH}$	$I_{OH} = -4.0mA$	2.4	-	-	V

Typical values are at  $V_{CC}=5.0V, T_A=25^\circ C$  and specified loading.

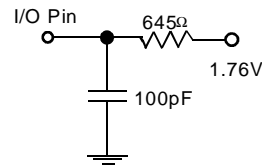
**Capacitance** ( $V_{CC}=5V\pm 10\%, T_A=25^\circ C$ )

Note: Capacitance calculated, not measured.

Parameter	Symbol	Test Condition	max	Unit
Input Capacitance (Address, $\overline{OE}$ , $\overline{WE}$ )	$C_{IN1}$	$V_{IN} = 0V$	32	pF
I/P Capacitance (other)	$C_{IN2}$	$V_{IN} = 0V$	8	pF
I/O Capacitance	$C_{IO}$	$V_{IO} = 0V$	32	pF

**AC Test Conditions****Output Load**

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: see diagram
- \*  $V_{CC} = 5V \pm 10\%$

**Operation Truth Table**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	High Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	Standby
L	L	H	Data Out	$I_{CC1}$	Read
L	H	L	Data In	$I_{CC1}$	Write
L	L	L	Data In	$I_{CC1}$	Write
L	H	H	High-Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	High-Z

Notes : H =  $V_{IH}$  : L =  $V_{IL}$  : X =  $V_{IH}$  or  $V_{IL}$

**Low  $V_{CC}$  Data Retention Characteristics - L Version Only**

Parameter	Symbol	Test Condition	min	typ <sup>(1)</sup>	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current		$V_{CC} = 3.0V, \overline{CS} \geq V_{CC} - 0.2V$				
	$I_{CCDR2}$	$T_{OP} = 0$ to $70^{\circ}C$	-	-	2	mA
Chip Deselect to Data Retention Time	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_r$	See Retention Waveform	5	-	-	ms

- Notes (1) Typical figures are measured at 25°C.  
 (2) This parameter is guaranteed not tested.

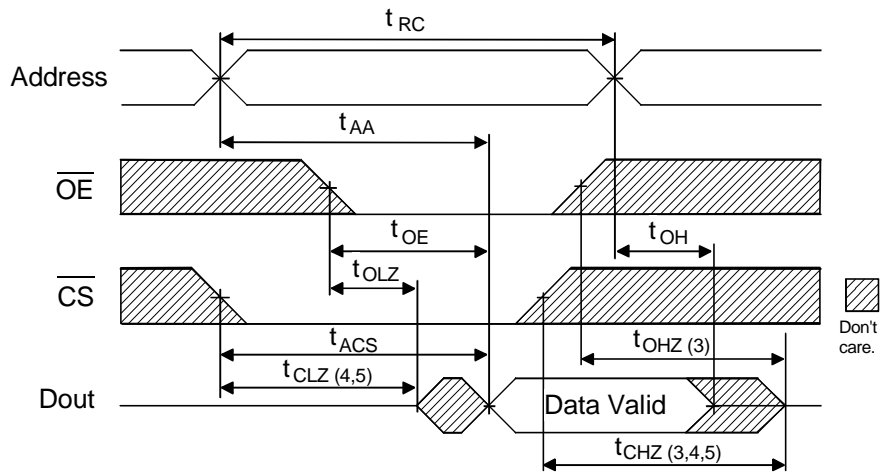
**AC OPERATING CONDITIONS****Read Cycle**

<i>Parameter</i>	<i>Symbol</i>	<i>-20</i>		<i>-25</i>		<i>-35</i>		<i>-45</i>		<i>Unit</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Read Cycle Time	$t_{RC}$	20	-	25	-	35	-	45	-	ns
Address Access Time	$t_{AA}$	-	20	-	25	-	35	-	45	ns
Chip Select Access Time	$t_{ACS}$	-	20	-	25	-	35	-	45	ns
Output Enable to Output Valid	$t_{OE}$	-	10	-	13	-	15	-	20	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	$t_{CLZ}$	0	-	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	$t_{CHZ}$	0	12	0	15	0	15	0	20	ns
Output Disable to Output in High Z	$t_{OHZ}$	0	10	0	12	0	20	0	20	ns

**Write Cycle**

<i>Parameter</i>	<i>Symbol</i>	<i>-20</i>		<i>-25</i>		<i>-35</i>		<i>-45</i>		<i>Unit</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Write Cycle Time	$t_{WC}$	20	-	25	-	35	-	45	-	ns
Chip Selection to End of Write	$t_{CW}$	17	-	20	-	30	-	40	-	ns
Address Valid to End of Write	$t_{AW}$	17	-	20	-	30	-	40	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	15	-	20	-	30	-	30	-	ns
Write Recovery Time	$t_{WR}$	3	-	3	-	3	-	3	-	ns
Write to Output in High Z	$t_{WHZ}$	0	12	0	15	0	15	0	15	ns
Data to Write Time Overlap	$t_{DW}$	12	-	15	-	20	-	25	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Output active from end of write	$t_{OW}$	0	-	0	-	0	-	0	-	ns

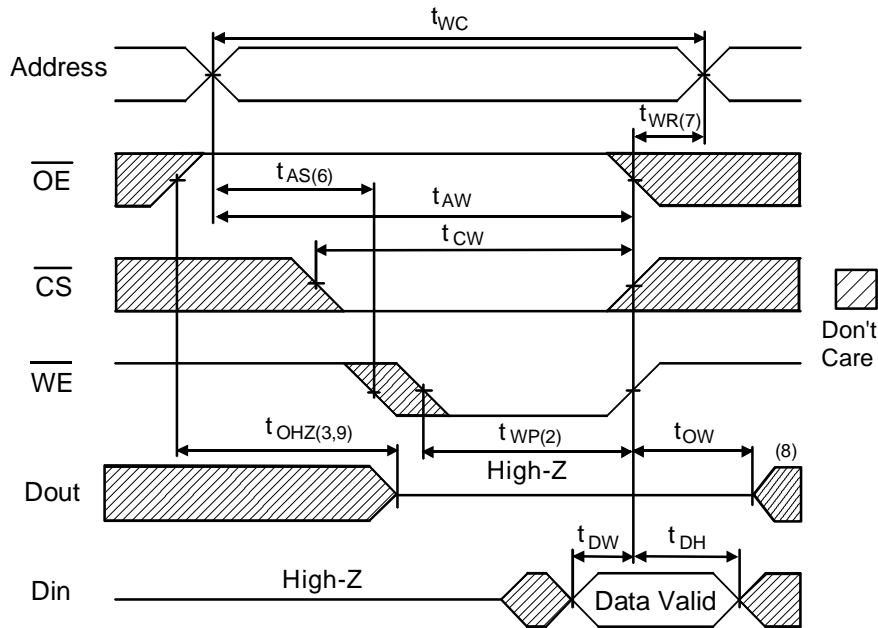
**Read Cycle Timing Waveform** <sup>(1,2)</sup>



**AC Read Characteristics Notes**

- (1)  $\overline{WE}$  is High for Read Cycle.
- (2) All read cycle timing is referenced from the last valid address to the first transition address.
- (3)  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
- (4) At any given temperature and voltage condition,  $t_{CHZ}$  (max) is less than  $t_{CLZ}$  (min) both for a given module and from module to module.
- (5) These parameters are sampled and not 100% tested.

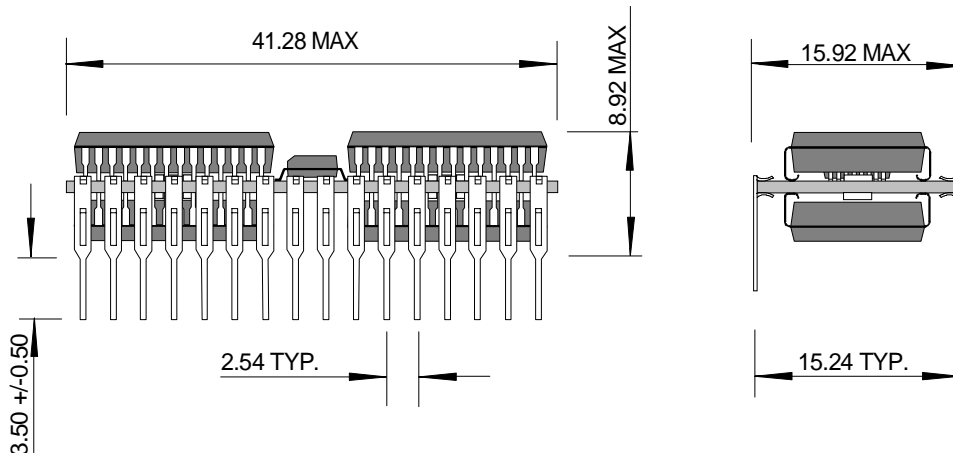
**Write Cycle No.1 Timing Waveform** <sup>(1,4)</sup>





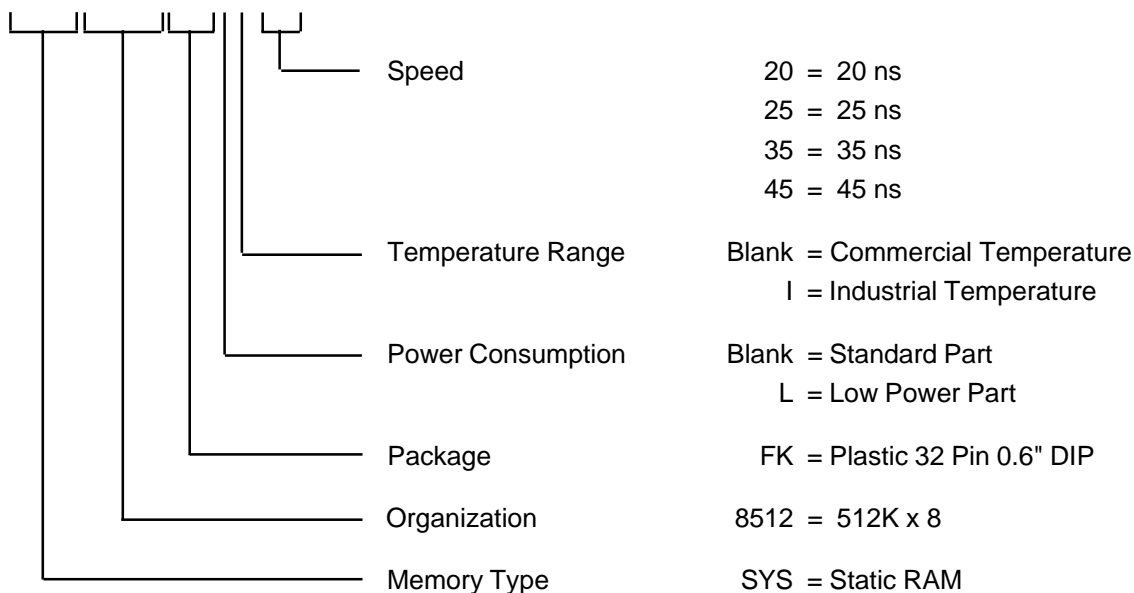
**Package Information** (Dimensions in Millimetres)

**Plastic 32 Pin 0.6" Dual-in-Line**



**Ordering Information**

**SYS8512FKLI-20**



**Note :**

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