

# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES



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## 256K x 32 SRAM MODULE

### PUMA 68SV8000X - 012/015/020

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#### Description

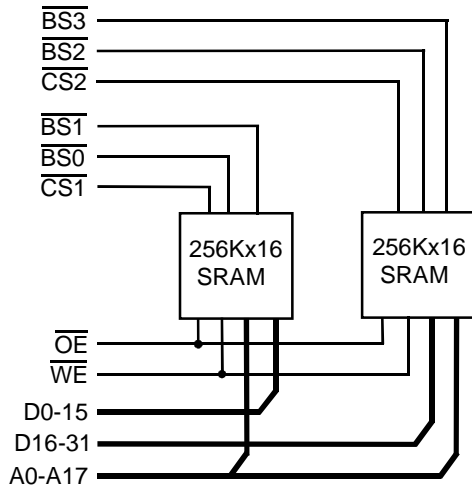
The PUMA 68SV8000X is a 3.3V 8Mbit CMOS High Speed Static RAM organised as 256Kx32 in a JEDEC 68 pin surface mount PLCC, available with access times of 12, 15, or 20ns. The output width is user configurable as 16 or 32 bits using two Chip Selects ( $\overline{CS1-2}$ ). 8-bit accessibility is achieved using four byte select pins ( $\overline{BS0-3}$ ).

The device features low power standby, multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 68SV8000X offers a dramatic space saving advantage over two standard 256Kx16 devices. The PUMA 68SV8000X is a pin compatible upgrade path from the PUMA 68SV2000X.

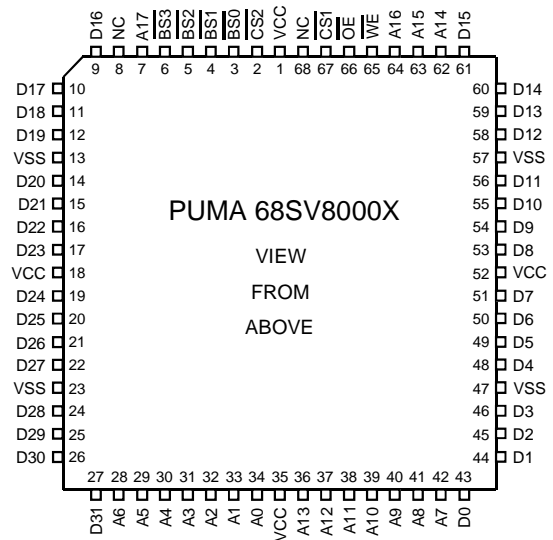
#### Features

- Very Fast Access Times of 12/15/20 ns.
- JEDEC 68 'J' leaded plastic Surface Mount Substrate.
- User Configurable as 16 / 32 bit wide output.
- Operating Power : 1.80 W (Max)  
Standby Power (TTL) : 1.12 W (Max)  
(CMOS) : 432 mW (Max)
- Individual byte enables provide byte accessibility.
- TTL Compatible Inputs and Outputs.
- Fully Static operation.
- Multiple ground pins for maximum noise immunity.
- Single 3.3V±10% Power supply.

#### Block Diagram



#### Pin Definition



#### Pin Functions

Address Inputs	<b>A0 - A17</b>
Data Input/Output	<b>D0 - D31</b>
Chip Select	<b><math>\overline{CS1-2}</math></b>
Byte Select	<b><math>\overline{BS0-3}</math></b>
Write Enable	<b><math>\overline{WE}</math></b>
Output Enable	<b><math>\overline{OE}</math></b>
No Connect	<b>NC</b>
Power (+3.3V)	<b>V<sub>cc</sub></b>
Ground	<b>GND</b>

#### Package Details

Plastic 68 J-Leaded JEDEC PLCC

**DC OPERATING CONDITIONS**

**Absolute Maximum Ratings <sup>(1)</sup>**

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub> <sup>(2)</sup>	-0.3	-	4.6	V
Power Dissipation	P <sub>T</sub>	-	-	2.0	W
Storage Temperature	T <sub>STG</sub>	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V<sub>T</sub> can be -2.0V pulse of less than 10ns.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V	
Operating Temperature	(Commercial)	T <sub>A</sub>	0	-	70	°C
	(Industrial)	T <sub>AI</sub>	-40	-	85	°C

**DC Electrical Characteristics (V<sub>CC</sub>=3.3V±10%) TA 0 to 70 °C**

Parameter	Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current	I <sub>LI</sub>	Address, $\overline{OE}, \overline{WE}$ 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-4	-	4	µA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS1-2} = V_{IH}, V_{I/O} = GND \text{ to } V_{CC}$	-4	-	4	µA
Operating Supply Current	32-bit mode	I <sub>CC1</sub> Min. Cycle, $\overline{CS1-2} = V_{IL}, V_{IL} \leq V_{IN} \leq V_{CC} - 2.1V$ $\overline{BS0-3} = V_{IL}$	-	-	500	mA
	16-bit mode	I <sub>CC2</sub> Min. Cycle, $\overline{BS0-3} = V_{IL}, V_{IL} \leq V_{IN} \leq V_{CC} - 2.1V,$ $\overline{CS1} = V_{IL} \text{ or } \overline{CS2} = V_{IL}.$	-	-	310	mA
Standby Supply Current	TTL levels	I <sub>SB1</sub> $\overline{CS1-2} = V_{IH}$	-	-	120	mA
	CMOS levels	I <sub>SB2</sub> $\overline{CS1-2} \geq V_{CC} - 0.2V, 0.2 \leq V_{IN} \leq V_{CC} - 0.2V$	-	-	20	mA
Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	-	-	0.4	V
	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	-	-	V

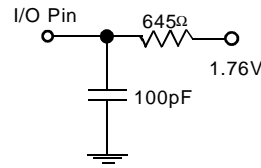
Typical values are at V<sub>CC</sub>=3.3V, T<sub>A</sub>=25°C and specified loading.

**Capacitance (V<sub>CC</sub>=3.3V±10%, T<sub>A</sub>=25°C)** Note: Capacitance calculated, not measured.

Parameter	Symbol	Test Condition	max	Unit
Input Capacitance (Address, $\overline{OE}, \overline{WE}$ )	C <sub>IN1</sub>	V <sub>IN</sub> = 0V	20	pF
I/P Capacitance (other)	C <sub>IN2</sub>	V <sub>IN</sub> = 0V	13	pF
I/O Capacitance (16-bit Mode - worst case)	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	22	pF

**AC Test Conditions** **Output Load**

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 3ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: see diagram
- \*  $V_{CC} = 3.3V \pm 10\%$



**Operation Truth Table**

$\overline{CS1}$	$\overline{CS2}$	$\overline{BS0}$	$\overline{BS1}$	$\overline{BS2}$	$\overline{BS3}$	$\overline{OE}$	$\overline{WE}$	SUPPLY CURRENT	MODE
L	L	L	H	H	H	X	L	Icc1	Write D0-7
L	L	H	L	H	H	X	L	Icc1	Write D8-15
L	L	H	H	L	H	X	L	Icc1	Write D16-23
L	L	H	H	H	L	X	L	Icc1	Write D24-31
L	L	L	L	H	H	X	L	Icc1	Write D0-15
L	L	H	H	L	L	X	L	Icc1	Write D16-31
L	L	L	L	L	L	X	L	Icc1	Write D0-31
L	L	H	H	H	H	X	L	Icc1	D0-31 High-Z
L	L	L	H	H	H	L	H	Icc1	Read D0-7
L	L	H	L	H	H	L	H	Icc1	Read D8-15
L	L	H	H	L	H	L	H	Icc1	Read D16-23
L	L	H	H	H	L	L	H	Icc1	Read D24-31
L	L	L	L	H	H	L	H	Icc1	Read D0-15
L	L	H	H	L	L	L	H	Icc1	Read D16-31
L	L	L	L	L	L	L	H	Icc1	Read D0-31
L	L	X	X	X	X	H	H	Icc1	D0-31 High-Z
L	H	L	L	X	X	X	L	Icc2	Write D0-15, D16-31 Standby
L	H	L	H	X	X	X	L	Icc2	Write D0-7, D16-31 Standby
L	H	H	L	X	X	X	L	Icc2	Write D8-15, D16-31 Standby
L	H	H	H	X	X	X	L	Icc2	D0-15 High-Z, D16-31 Standby
L	H	X	X	X	X	H	H	Icc2	D0-15 High-Z, D16-31 Standby
H	L	X	X	L	L	X	L	Icc2	D0-15 Standby, Write D16-31
H	L	X	X	L	H	X	L	Icc2	D0-15 Standby, Write D16-23
H	L	X	X	H	L	X	L	Icc2	D0-15 Standby, Write D24-31
H	L	X	X	H	H	X	L	Icc2	D0-15 Standby, D16-31 High-Z
H	L	X	X	X	X	H	H	Icc2	D0-15 Standby, D16-31 High-Z
H	H	X	X	X	X	X	X	ISB1, ISB2	D0-31 Standby

Notes : H =  $V_{IH}$  : L =  $V_{IL}$  : X =  $V_{IH}$  or  $V_{IL}$

## AC OPERATING CONDITIONS

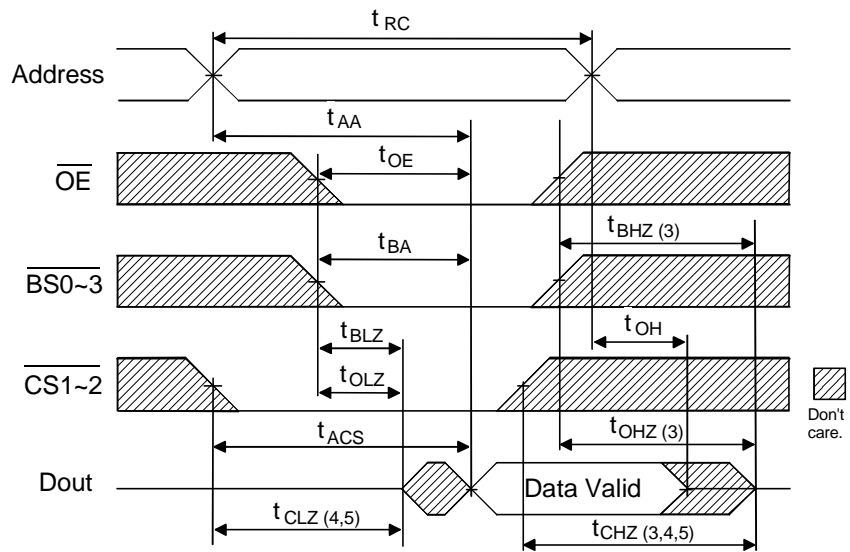
### Read Cycle

Parameter	Symbol	-012		-015		-020		Unit
		min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	12	-	15	-	20	-	ns
Address Access Time	$t_{AA}$	-	12	-	15	-	20	ns
Chip Select Access Time	$t_{ACS}$	-	12	-	15	-	20	ns
Byte Select Access Time	$t_{BA}$	-	6	-	7	-	10	ns
Output Enable to Output Valid	$t_{OE}$	-	6	-	7	-	10	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	$t_{CLZ}$	3	-	3	-	3	-	ns
Byte Selection to Output in Low Z	$t_{BLZ}$	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	$t_{CHZ}$	0	6	0	7	0	9	ns
Output Disable to Output in High Z	$t_{OHZ}$	0	6	0	7	0	9	ns
Byte Deselection to Output in High Z	$t_{BHZ}$	0	6	0	7	0	9	ns

### Write Cycle

Parameter	Symbol	-012		-015		-020		Unit
		min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	12	-	15	-	20	-	ns
Chip Selection to End of Write	$t_{CW}$	10	-	12	-	15	-	ns
Byte Selection to End of Write	$t_{BW}$	10	-	12	-	15	-	ns
Address Valid to End of Write	$t_{AW}$	10	-	12	-	15	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	10	-	12	-	15	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Write to Output in High Z	$t_{WHZ}$	0	6	0	7	0	9	ns
Data to Write Time Overlap	$t_{DW}$	7	-	8	-	10	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Output active from end of write	$t_{OW}$	3	-	3	-	3	-	ns

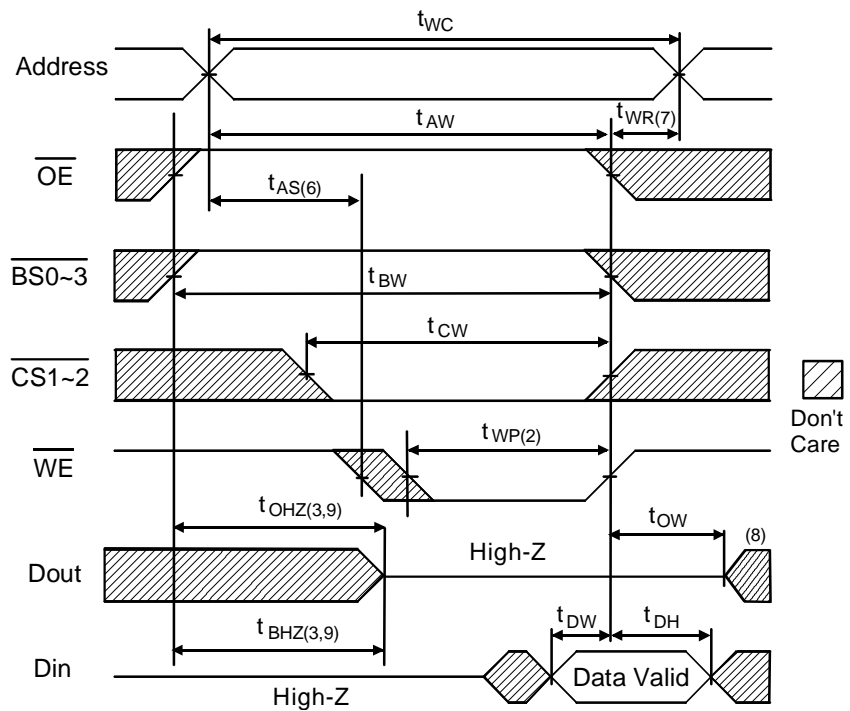
**Read Cycle Timing Waveform** <sup>(1,2)</sup>



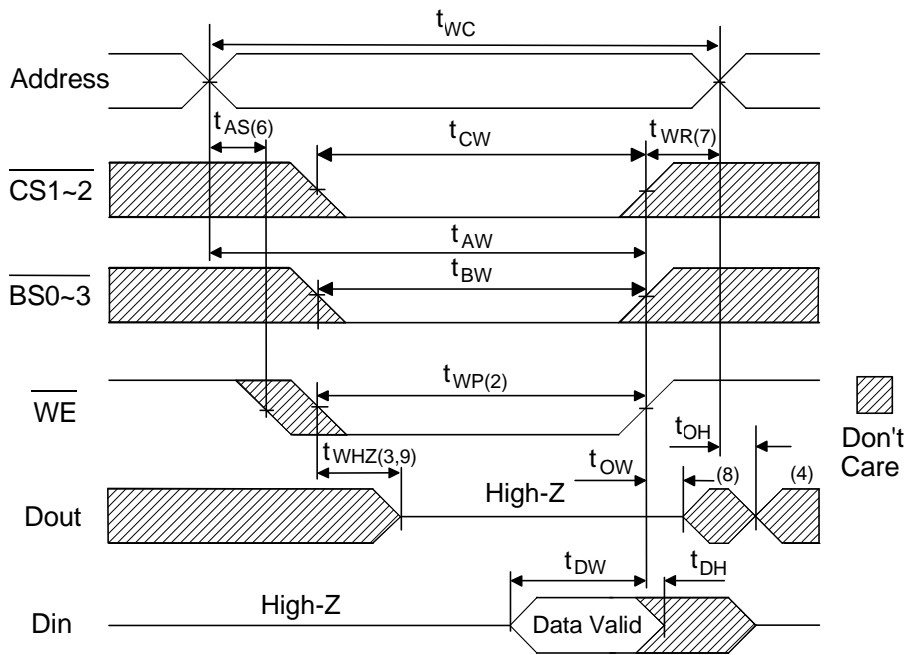
**AC Read Characteristics Notes**

- (1)  $\overline{WE}$  is High for Read Cycle.
- (2) All read cycle timing is referenced from the last valid address to the first transition address.
- (3)  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
- (4) At any given temperature and voltage condition,  $t_{CHZ}$  (max) is less than  $t_{CLZ}$  (min) both for a given module and from module to module.
- (5) These parameters are sampled and not 100% tested.

**Write Cycle No.1 Timing Waveform** <sup>(1,4)</sup>



**Write Cycle No.2 Timing Waveform <sup>(1,5)</sup>**

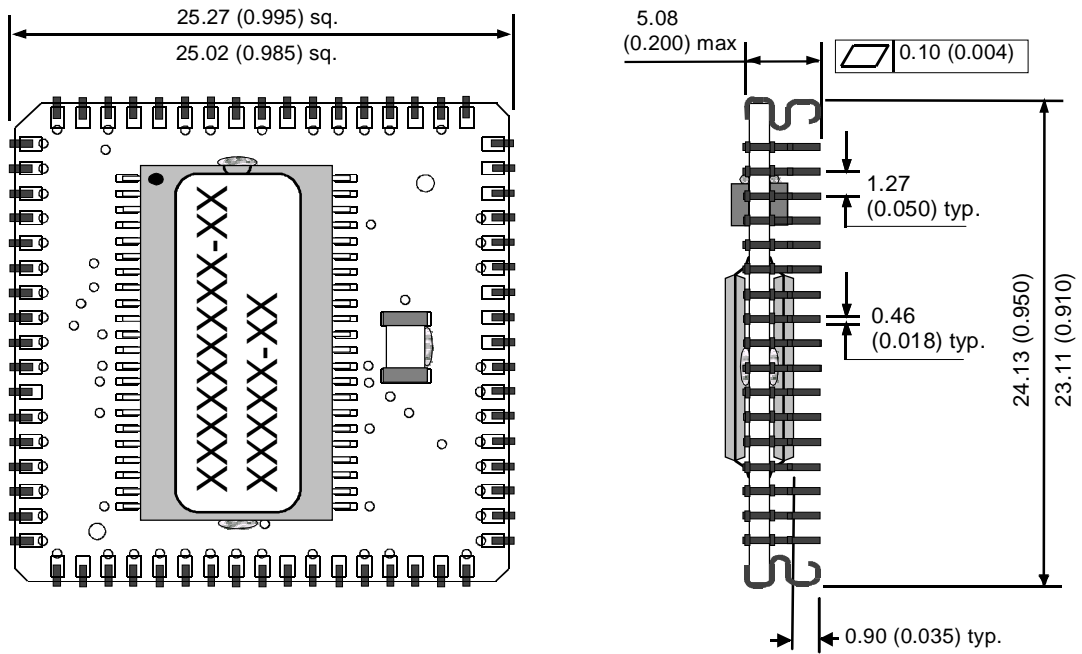


**AC Write Characteristics Notes**

- (1) All write cycle timing is referenced from the last valid address to the first transition address.
- (2) All writes occur during the overlap of  $\overline{CS1\sim2}$ ,  $\overline{BS0\sim3}$  and  $\overline{WE}$  low.
- (3) If  $\overline{OE}$ ,  $\overline{CS1\sim2}$ ,  $\overline{BS0\sim3}$ , and  $\overline{WE}$  are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
- (4) Dout is the Read data of the new address.
- (5)  $\overline{OE}$  is continuously low.
- (6) Address is valid prior to or coincident with  $\overline{CS1\sim2}$ ,  $\overline{BS0\sim3}$  and  $\overline{WE}$  low, too avoid inadvertant writes.
- (7)  $\overline{CS1\sim2}$ ,  $\overline{BS0\sim3}$  or  $\overline{WE}$  must be high during address transitions.
- (8) When  $\overline{CS1\sim2}$  and  $\overline{BS0\sim3}$  are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
- (9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

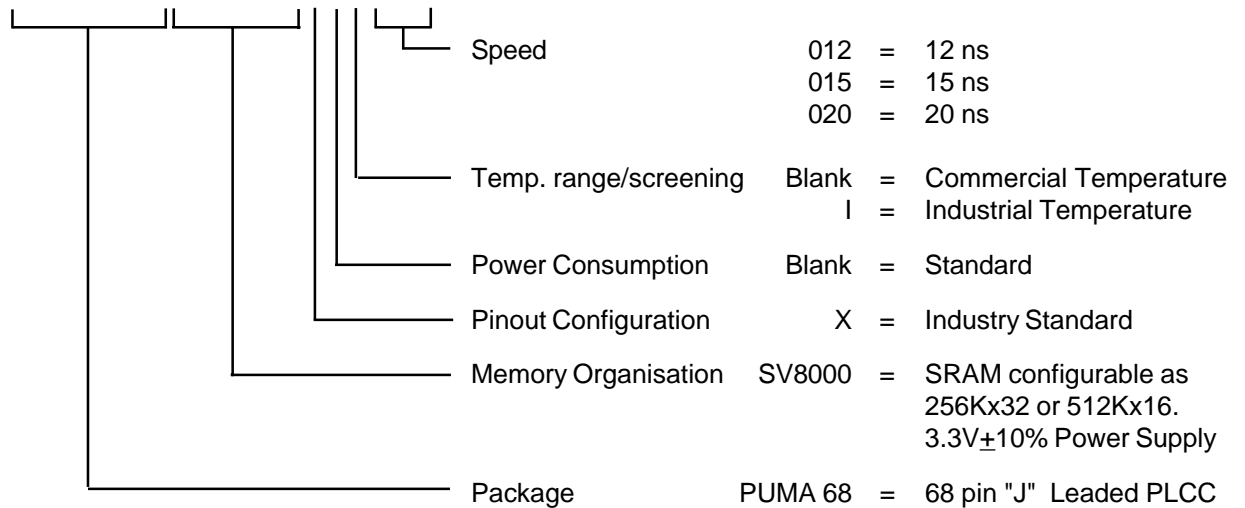
**Package Information**    Dimensions in mm(inches)

**Plastic 68 Pin JEDEC Surface mount PLCC**



**Ordering Information**

**PUMA 68SV8000XLI-012**



## Moisture Sensitivity

Devices are **moisture sensitive**.

Shelf Life in Sealed Bag 12 months at <40°C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220°C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30°C/60% RH

**OR**

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23°C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125°C +/-5% for high temperature device containers

**OR**

B : 192 hours at 40°C +5°C/-0°C and <5% RH for low temperature device containers.

## Soldering Recommendations

IR/Convection -	Ramp Rate	6°C/sec max.
	Temp. exceeding 183°C	150 secs. max.
	Peak Temperature	225°C
	Time within 5°C of peak	20 secs max.
	Ramp down	6°C/sec max.
Vapour Phase -	Ramp up rate	6°C/sec max.
	Peak Temperature	215 - 219°C
	Time within 5°C of peak	60 secs max.
	Ramp down	6°C/sec max.

The above conditions must not be exceeded

*Note : The above recommendations are based on standard industry practice. Failure to comply with the above recommendations invalidates product warranty.*

Note :

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.